mulation-type trench gate structure MOSFET, controlling a voltage applied to the gate electrode results in a control of a channel formed in a first electrically conductive type channel layer between the sidewall of the trench and the base region. This allows an electric current to flow between the first and second electrodes via the source region and the drift layer.

[0013] The SiC semiconductor device may preferably further include, for instance, second electrically conductive type contact regions, spaced in placement from the trench so as to sandwich the source region to allow the base regions to be electrically connected to the first electrode, each of which has a higher concentration than that of the base region. In this case, the deep layer is placed beneath the contact region to be unitarily formed with the contact region. The deep layer has a second electrically conductive type impurity concentration ranging from, for instance, $1.0\times10^{17}/cm^3$ to $1.0\times10^{20}/cm^3$. Further, the deep layer may be preferably arranged to have a depth of, for instance, 1.5 to 3.5 μm from a surface of the base region.

[0014] The SiC semiconductor device may preferably further comprise a second electrically conductive type reserve layer, formed on the drift layer in an area below the trench and the deep layer, which has a lower concentration than that of the deep layer.

[0015] With such a reserve layer being provided, an electric field of an area beneath the trench can be further reduced, enabling further improved effects to be obtained.

[0016] The SiC semiconductor device may preferably further comprise a first electrically conductive type low resistance region, formed in an area between the sidewall of the trench and the deep layer, which has a higher concentration than that of the drift layer.

[0017] With such a low resistance region being provided, the drift layer can have further lowered resistance, enabling a reduction on resistance. Such a low resistance region may be provided not only in the area between the sidewall of the trench and the deep layer but also in an area between the sidewall of the trench and the reserve layer.

[0018] Although the above description has been directed to the case in which the deep layer is provided, further, the deep layer may be replaced by a metallic layer that cooperates with the drift layer to provide a structure acting as a Schockley diode. With such a Schockley diode having a fast reacting speed being provided, the SiC semiconductor device can be formed in a structure with an increased withstand surge voltage.

[0019] The SiC semiconductor device can be manufactured in a method as described below.

[0020] For instance, the method of manufacturing the SiC semiconductor device comprises the steps of: preparing a first or second electrically conductive type substrate made of 4H SiC and having a surface on a (000-1) c-plane or a (0001) Si-plane; forming a drift layer on the substrate with the first electrically conductive type SiC with a lower impurity concentration that that of the substrate; forming a base region on the drift layer by ion-implanting a second electrically conductive type impurity in a given position spaced from a surface of the drift layer; forming a source region with the first electrically conductive type SiC with a higher concentration than that of the drift layer by ion-implanting a first electrically conductive type impurity on a surface layer portion of the base region in an area within the base region; forming a trench-gate forming trench in an area penetrating a surface of the drift layer to pass through the source region and the base region to reach the drift layer and including a sidewall having a surface extending in a [11-20] direction or a [1-100] direction; forming a deep-layer forming trench in an area spaced from the trench-gate forming trench by a given distance and having a depth equal to or greater than that of the trench-gate forming trench; infilling the deep-layer forming trench with a second electrically conductive type deep layer with a higher concentration than that of the base region; forming a gate oxide film over a surface of the trench-gate forming trench by thermal oxidation; forming a gate electrode on the gate oxide film in the trench-gate forming trench; forming a first electrode electrically in electrical connection to the source region; and forming a second electrode on the substrate at a rear surface thereof. Such a method enables the SiC semiconductor device of the inversion-type trench gate structure to be manufactured.

[0021] During the step of forming the base region, further, a plurality of base regions are formed at positions each spaced from the sidewall of the trench by a given distance. In addition, during the step of forming the trench-gate forming trench, the trench-gate forming trench is formed in an area between the plural base regions. The trench-gate forming trench is formed so as to extend from a surface of the drift layer to an area deeper than the source region and the base region and spaced from the base regions by a given distance with the sidewall laying on a surface extending in the [11-20] direction or the [1-100] direction.

[0022] In these cases, the step of forming a trench-gate forming trench and the step of forming a deep-layer forming trench may preferably allow the trench-gate forming trench and the deep-layer forming trench to be simultaneously formed. With such steps being carried out, the trench forming steps can be simplified.

[0023] With the method of manufacturing the SiC semiconductor device, before infilling the deep layer after forming the trench-gate forming trench and the deep-layer forming trench, a second electrically conductive impurity may be preferably ion implanted onto bottom walls of the trench-gate forming trench and the deep-layer forming trench. This allows a reserve layer to be formed with a lower concentration than that of the deep layer.

[0024] Further, during the step of forming the drift layer, a step may be preferably carried out for forming a first electrically conductive type low resistance region in an area deeper than the base region with the drift layer having a high concentration. During the step of forming the low resistance region, the low resistance region may be preferably formed in a position between the trench-gate forming trench and the deep layer. This allows the drift layer to have lowered resistance, thereby enabling a reduction in on resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] FIG. **1** is a cross-sectional view of a MOSFET of an inversion-type trench gate structure of a first embodiment according to the present invention.

[0026] FIGS. **2**A to **2**C are cross-sectional views showing how the trench gate type MOSFET, shown in FIG. **1**, is manufactured.

[0027] FIGS. **3**A to **3**C are cross-sectional views showing other steps, subsequent to the steps shown in FIGS. **2**A to **2**C, for manufacturing the trench gate type MOSFET shown in FIG. **1**.